WHAT IS CLAIMED IS:

1. A programmable, single chip embedded processor system for input/output applications, comprising:

a modular, multiple bit, multithread processor core operable by at least four parallel and independent application threads sharing common execution logic segmented into a multiple stage processor pipeline, wherein said processor core is capable of having at least two states;

a logic mechanism engaged with said processor core for executing an instruction set within said processor core;

a supervisory control unit, controlled by at least one of said processor core threads, for examining said core processor state and for controlling said core processor operation;

a memory for storing and executing said instruction set data; and

a peripheral adaptor engaged with said processor core for transmitting input/output signals to and from said processor core.

2. A system as recited in Claim 1, wherein said processor pipeline includes an instruction fetch logic stage, instruction decode logic stage, multiple port register read stage, address mode logic stage, arithmetic logic unit for arithmetic and address calculations stage, multiple port memory stage, branch/wait logic stage and multiple port register write stage.

3. A system as recited in Claim 1, wherein said processor core supports "n" multiple groups of independent threads by replicating said common execution logic and said memory.

4. A system as recited in Claim 1, further comprising a condition code mechanism implemented in said instruction set for detecting specific word data types.

5. A system as recited in Claim 4, wherein the value of the least significant byte of a word is detected to be within a specific range.

6. A system as recited in Claim 1, wherein said instruction set includes a processor instruction for enabling individual threads to determine their thread identity.

7. A system as recited in Claim 1, wherein said supervisory control unit is capable of examining and interpreting the state of multithread processor core operation for the purpose of starting, stopping, and modifying individual multithread processor operation.

8. A system as recited in Claim 7, further comprising a hardware semaphone vector engaged with said supervisory control unit for controlling multithread access to said peripheral and system memory.

9. A system as recited in Claim 1, wherein said supervisory control unit is capable of being accessed and controlled by each of said operating core processor threads by using input/output instructions.

10. A system as recited in Claim 9, wherein said controlling operating processor thread is programmable and comprises any of the available threads.

11. A system as recited in Claim 9, wherein said controlling operating core processor thread is capable of reconfiguring the overall thread processing method of operation so that other processing threads can support multiple instruction multiple data processing operations.

12. A system as recited in Claim 9, wherein said controlling operating processor thread can reconfigure the overall thread processing method of operation so that other processing threads can support single instruction multiple data processing operations.

13. A system as recited in Claim 9, wherein said controlling operating processor thread is capable of reconfiguring the overall thread processing method of operation so that an arbitrary number of processing threads can support simultaneously single instruction multiple data processing operations and multiple instruction multiple data processing operations.

14. A system as recited in Claim 1, wherein said supervisory control unit is operable by a first thread process to start and stop another thread process and to examine and alter state information in single step and multiple step modes of controlled operation.

15. A system as recited in Claim 1, further comprising identifying bit patterns embedded in the unassigned bit fields of the machine instructions of said core processor.

16. A system as recited in Claim 1, wherein said memory comprises internal memory for storing and executing core processor code and external memory engaged with said peripheral adaptor.

17. A system as recited in Claim 1, wherein said supervisory control unit is configured as a peripheral to said processor core.

18. A system as recited in Claim 1, wherein said peripheral adaptor is capable of controlling analog and digital processing functions.